AMD FINANCIAL ANALYST DAY NEWS SUMMARY
DECEMBER 13, 2007

Earlier today, AMD held its annual Financial Analyst Day at the New York Stock Exchange in New York City. The event was hosted by members of the AMD executive team, and featured presentations and news disclosures that provided key updates on AMD business, financials and technology.

As AMD Chairman and CEO Hector Ruiz said today during his presentation, today's event was not just about how AMD is preparing for the future, but how the company is dealing with challenges in the present. There is incredible opportunity ahead for AMD products and technology. Customer demand is strong and the company expects to see increased momentum across all major dimensions of AMD business. Each AMD business unit is entering an exciting new product cycle – from panel processors in the digital television space to high performance quad-core processors to a next-generation notebook platform. The opportunity is now and AMD is prepared to deliver.

Below is a summary of key highlights and disclosures from the event. A press-only recap and Q&A session will be held shortly. Please join this session for additional insight into today's event.

AMD FINANCIAL ANALYST DAY: EXECUTIVE SUMMARY

Corporate Priorities

- AMD plans to continue delivering differentiated platform solutions, driving growth opportunities for our customers.
- AMD is focused on volume and revenue "sweet spots," delivering high-end performance to the mainstream.
- AMD is working to achieve profitability in each of our businesses for 2008.

Computing Products

- The 2008-2009 roadmap overview includes several updates:
    - Initial shipments of the updated Quad-Core AMD Opteron processors are planned for Q108. Platforms from AMD OEM and system builder partners are expected in Q208.
    - "Montreal" will be AMD's first octal-core server processor in 2009, and will be introduced in tandem with the first AMD server platform, codenamed "Piranha." In addition to featuring a new AMD server chipset, the "Piranha" multi-processor platform will feature HyperTransport™ 3.0 and DDR3 memory technology.
    - AMD detailed its first notebook APU, codenamed "Swift," and first APU-based notebook platform, codenamed "Shrike." "Swift" will use existing CPU core and GPU core technologies, integrated on a single silicon die.
    - The "Shrike" platform is planned to benefit from the faster data throughput and greater power efficiency of the "Swift" APU design to deliver richer graphics, a better digital media experience, improved overall performance, and longer battery life for users. AMD plans to ship "Swift" and "Shrike" in time to enable customers to begin volume sales of "Shrike"-based platforms in second half 2009.

Graphics Products

- AMD shared details about its successful transition to 55nm with a top-to-bottom portfolio of graphics processors in early 2008.
- AMD expects to achieve a comprehensive multi-GPU leadership position with CrossFireX for enthusiasts and Hybrid Graphics for entry-level and mainstream users.
- ATI graphics continue to be the choice of customers for AMD and competitive platform transitions. AMD expects to achieve notebook discrete graphics design win leadership in 2008.

Consumer Electronics

- AMD sees big opportunities for growth in its consumer electronics business. Key market drivers for AMD momentum in this space include:
    - TV sales are rapidly shifting to LCD TVs with larger displays and higher resolutions that require better video quality; AMD is #1 in MPEG Video Processors (according to DisplaySearch) and has new products in the pipeline that will continue to deliver better image quality and performance.
    - Handset graphics technology is driving the user experience with the emergence of touch screen user interfaces; AMD offers leading 3-D graphics and the industry's first hardware 2-D vector graphics.

Manufacturing Priorities

- AMD internal manufacturing capability remains world-class.
- The company is on schedule for the ramp of 45nm in first half of 2008, with products in market during second half of 2008.
- The AMD technology development alliance with IBM continues to deliver: First 32nm SRAMs were demonstrated; plan continues for 2010 introduction of 32nm parts.

ADDENDUM: DEFINITIONS

Accelerated Computing

Accelerated Computing represents both an AMD vision for the industry as well as a set of internal AMD R&D initiatives to achieve that vision. It focuses on enabling the integration of differing on-system accelerator chips and on-silicon accelerator cores, in varying configurations, to achieve greater performance, higher energy efficiency and improved functionality.

Today, AMD's Accelerated Computing technology initiative is broken into three primary parts, with each sub-initiative focused on enabling one of the critical aspects of the overall Accelerated Computing vision: "Torrenza," "Fusion," and "Bedrock."

Accelerated Processing Units (APUs)

Primarily as a result of the AMD "Fusion" efforts, AMD will introduce a new category of microprocessor called the Accelerated Processing Unit (APU). APUs are individualized processor designs, mixing various combinations of CPU cores and accelerator cores, targeted at specific market segments.

The first generation of APUs are planned for release in second half 2009 and will be x86 processors that integrate one or more processor cores with one or more graphics processor cores, requiring little to no changes in existing programming models or the

x86 ISA. Later, APU core diversity will increase, creating a nearly limitless variety of possible core and accelerator combinations, with increasing levels of value-delivery, based on the specific priorities of the respective end-user segment.

"Bedrock" Internal AMD R&D Initiative

This foundational initiative involves enabling and driving industry-friendly definition and wide adoption of standardized programming models that allow an increasingly diverse set of accelerator cores, including the full compute power of general-purpose GPUs, to be used in mainstream platforms.

"Fusion" Internal AMD R&D Initiative

"Fusion" is a set of silicon and system design programs focused on enabling varying accelerator cores be integrated on-silicon. Conceptually, silicon-level acceleration is somewhat similar to system-level acceleration, however increasing levels of speed and efficiency can be achieved through on-chip integration.

The first "Fusion"-based processor designs will primarily combine central processing unit (CPU) cores and graphics processing unit (GPU) cores on a single silicon die. Processing and visualization benefits will be largely achieved through reduced distance and material between processing cores, and therefore overall reduced data latency at reduced power.

In the future, differing types of cores will be integrated into "Fusion"-based designs. These designs will deliver even greater performance, energy-efficiency, and functionality for a growing variety of workloads/applications through evolving microarchitecture and software innovation.

"Torrenza" Internal AMD R&D Initiative

"Torrenza" is a set of hardware and ecosystem development programs focused on enabling separate, purpose-built chips created by AMD or by third parties to be attached to an AMD motherboard. These discrete accelerators offload specific types of work from the processor and process it at higher speed and efficiency than the processor is capable of alone.